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Original Research

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KEYWORDS:
CLA, Carry Skip Adder, Domino logic, CMOS

32-Bit Adder and Subtractor Using Multiple Output Domino Logic

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ABSTRACT: There is a huge scope for high-speed arithmetic units in VLSI. The proposed technique is for arithmetic operations like adder and subtractor which includes CLA (Carry Look Ahead), Carry Skip Adder techniques with Domino logic and usage of mux for faster computation and reduce the delay and complexity of the architecture. Cascaded CLA blocks are used here. 8 such structures are used here for faster computation. Mux is also used here for switching between the addition and subtraction operation. For high-speed performance and low delay, CMOS based domino logic is used here. The proposed design is less complex than other structures and has improved speed during its operation.

1. INTRODUCTION

The basic operation in digital system is ALU.

It mainly depends on speed of the operation.

To speed up the operation, here different adders are used namely RCA, CLA and CSA.

Ripple Carry Adder (RCA), is a low-speed computing adder. Carry Look-ahead Adder (CLA) is a fast-computing adder which generates carry parallelly. Carry Skip Adder reduces delay of computation in the blocks.

To reduce the delay and increase the speed of computation it is recommended to combine CLA and Carry Skip Adder, implementing domino logic, 2:1 Mux for selecting adder or subtraction and CMOS technology.

2. LITERATURE SURVEY

[1]. A comprehensive operand-aware dynamic clock gating scheme for low-power Domino Logic by Salim Farah, et.al, proposed domino logic scheme which uses the inactive portion of the functional units to save power.

[2]. Comparative delay, noise and energy of high-performance domino adders with stack node preconditioning (SNP) by Yibin Ye, proposed a method which has charge-sharing and noise reduction technique.

[3]. Power Reduction in Domino Logic using clock gating in 16nm CMOS Technology, by Smita Singhal .et.al., proposed clock gating and output holding technique to reduce power.

[4]. Comparator using Domino Logic and CMOS Logic by Abhishek V. Rangari, propsed a technique in which comparator is used as a reference circuit to reduce the consumption of power by 55% compared to CMOS technology in short circuit current flowing process.

[5]. An approach for detecting bridging faults in CMOS domino logic circuits using dynamic power supply current monitoring, by A Walker, e,al., proposed a technique for high to low(low to high) transition when power (or ground) is sourced(or sink) in an inverter.

[6]. Ultrafast compact 32-bit CMOS adders in multiple-output domino logic by I S Hwang proposed a technique which used CLA and rerduced the circuitry count by half and area and power are also reduced.

[7]. A Novel Technique to improve Performance Evaluation of Domino Logic Circuits in CMOS and FinFET Technology by Uday Panwar,et.al., proposed a design in wich eight and sixteen input OR gates are used with Fin-FET and CMOS technology.

[8]. Domino logic synthesis using complex static gates by T Thorp, et.al., proposed pairing of dynamic logic gate with any static inverter.

[9]. Design and Implementation of Domino Logic Circuit in CMOS by Ankita Sharma.et.al., proposed an analysis technique of different gates using domino logic.

3. METHODOLOGY

The different kinds of adders are implemented in this domino logic 32 bit adder and subtractor. CLA is used here.

CLA Adder

Carry Skip Adder

Carry Look-Ahead Adder

This adder is mainly used to reduce the delay during the computation process.

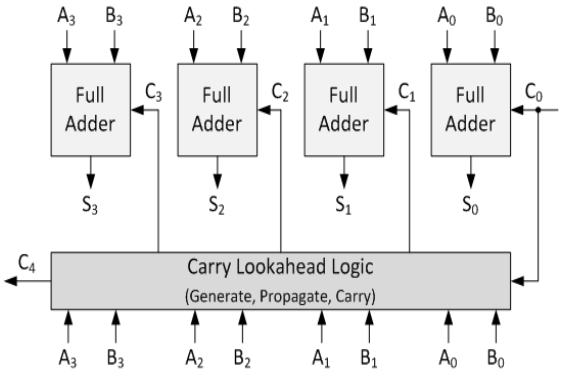


Fig.1 : General 4-bit carry look ahead adder

Here, Carry Generator and Carry Propagator are used. The carry generation can b computed in prior.

Considering a full adder, we can design as

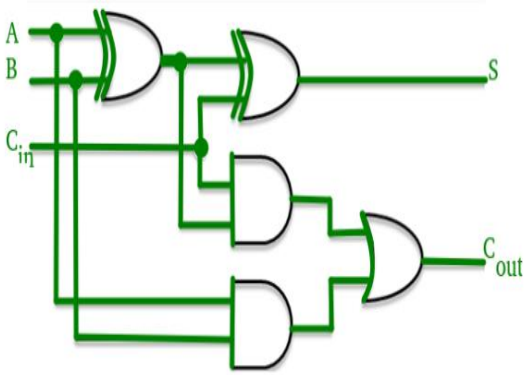


Fig 2: Full adder circuit diagram

For the above full adder circuit, the carry status can be calculated as follow.

Table 1: Carry generation with condition

A	B	C	C +1	Condition
0	0	0	0	No Carry Generate
0	0	1	0	
0	1	0	0	
0	1	1	1	No Carry Propogate
1	0	0	0	
1	0	1	1	
1	1	0	1	Carry Generate
1	1	1	1	

Carry Skip Adder

Carry look-ahead adder increases the speed of the circuit.

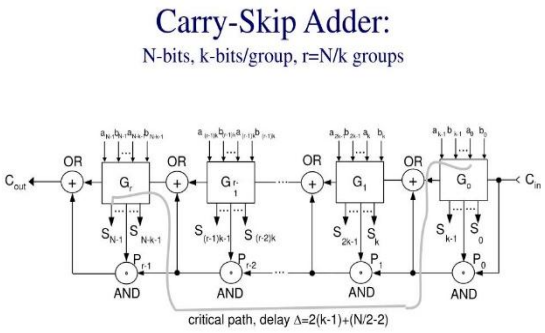


Fig 3: General Carry Skip Adder circuit

It skips based on consecutive adders and propagates the carry.it consumes less area and power. This adder is also called as Carry Bypass Adder.

CMOS Logic

CMOS logic consists of NMOS and PMOS

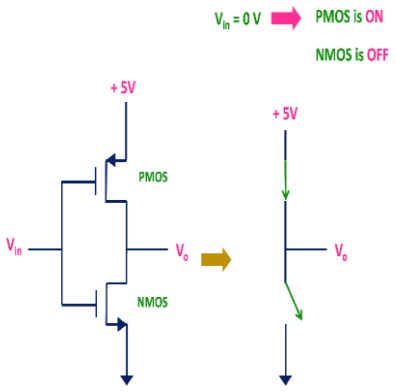


Fig .4 : Example of CMOS Inverter

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CMOS stands for Complementary Metal Oxide Semiconductor.

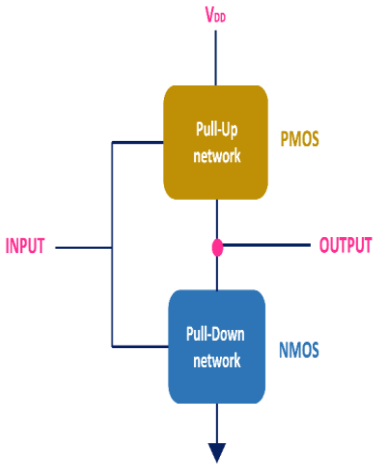


Fig. 5: CMOS Logic

PMOS is used as Pull-up network and NMOS is used as Pull-down network.

Multi-Output Domino Logic

In short form we call it as MODL Logic.

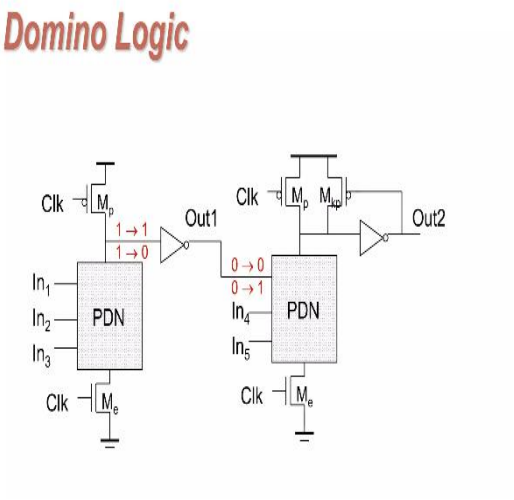


Fig. 6: Domino logic

The above diagram shows the domino logic.

Domino logic includes N+2 transistors and domino CMOS logic to remove the cascading problem.

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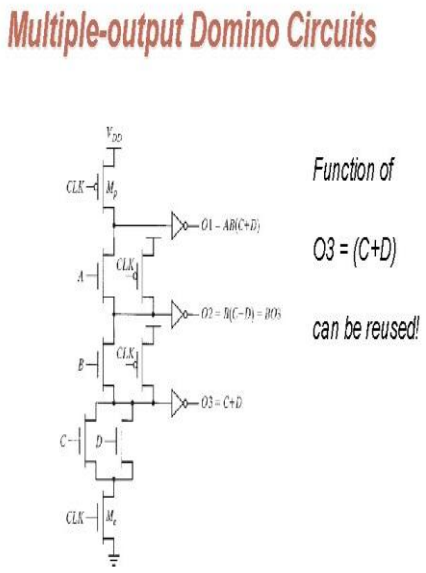


Fig.7: Multiple-Output Domino Logic

It is a technique, where multiple logic functions are generated from a single pre-charged node. It reduces power, area and delay.

Mux

Mux behaves like a data selector. It selects adder or subtractor based on the select lines.

There are so many radix techniques available. Among them radix2 radix 4 radix 8 radix 16 and radix 32 are found.

Table 2: Summary of Radix with range

Radix	Bits processed/group	Signed digit range	Maximum multiple
Radix-2	1	−1 to +1	A
Radix-4	2	−2 to +2	2A
Radix-8	3	−4 to +4	4A
Radix-16	4	−8 to +8	8A
Radix-32	5	−16 to +16	16A

Radix 2 encoding bits:Each group has 1 bit

Radix-4 encoding table: Each radix 4 encoding bits has 2 bits grouped together.

Radix 8 encoding: Each digit has three binary bits

Radix 16 encoding table: For radix 16 each digit shows 4 binary bits

Radix 16 booth encoding: For signed radix 16 it ranges from -8 to +7.

Radix 32 encoding

Table 3: Each radix 32 has 5 bits grouped together.

Decimal	Radix-32	Binary (5-bit)
0	0	00000
1	1	00001
2	2	00010
3	3	00011
4	4	00100
5	5	00101
6	6	00110
7	7	00111
8	8	01000
9	9	01001
10	A	01010
11	B	01011
12	C	01100
13	D	01101
14	E	01110
15	F	01111
16	G	10000
17	H	10001
18	I	10010
19	J	10011
20	K	10100
21	L	10101
22	M	10110
23	N	10111
24	O	11000
25	P	11001

Decimal	Radix-32	Binary (5-bit)
26	Q	11010
27	R	11011
28	S	11100
29	T	11101
30	U	11110
31	V	11111

Table 4: Radix-32 booth encoding

It has range from -16 to +15

Binary Group	Decimal Value	Partial Product
00000	0	0 × A
00001	+1	+A
00010	+2	+2A
00011	+3	+3A
00100	+4	+4A
00101	+5	+5A
00110	+6	+6A
00111	+7	+7A
01000	+8	+8A
01001	+9	+9A
01010	+10	+10A
01011	+11	+11A
01100	+12	+12A
01101	+13	+13A
01110	+14	+14A
01111	+15	+15A
10000	−16	−16A

Binary Group	Decimal Value	Partial Product
10001	−15	−15A
10010	−14	−14A
10011	−13	−13A
10100	−12	−12A
10101	−11	−11A
10110	−10	−10A
10111	−9	−9A
11000	−8	−8A
11001	−7	−7A
11010	−6	−6A
11011	−5	−5A
11100	−4	−4A
11101	−3	−3A
11110	−2	−2A
11111	−1	−A

Proposed Methodology

The multi-output domino logic is implemented in an ALU operation for addition and subtraction. It includes adders like Carry Look Ahead Adder and Carry Skip Adder. To choose addition or subtraction operation, mux is used. Here 2:1 mux is used.

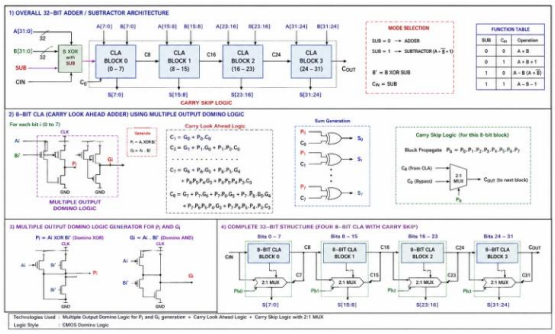


Fig.8: Block diagram of 32-bit adder is as shown in the figure

It consists of CLA Adder and multiplexers.

The carry is generated using multiple output domino logic for 8 bits.

Using these 8 bit carry, and multiplexer the parallel stages of CLA adder is implemented.

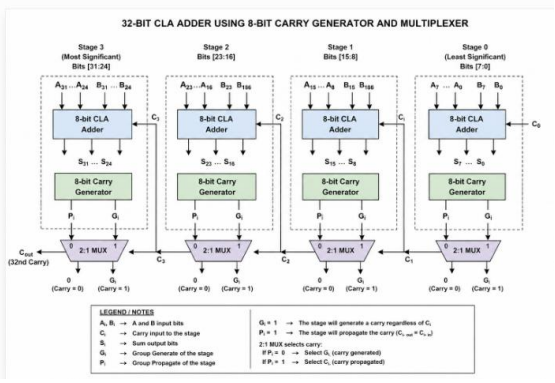


Fig. 9: Parallel stages of CLA adder with Multiplexer

The expression for 8 bit carry for CLA is as follows:

Carry generator and carry propagator can be defined as

Gi=Ai·Bi (Generate)

Pi=Ai⊕Bi (Propagate)

The sum and carry generator can be defined as

Si=Pi⊕Ci

$C_{i+1}=G_i+P_iC_i$

The next carry is propagated as C_{i+1}.

Here carry bits are generated.

C1=G0+P0C0

C2=G1+P1G0+P1P0C0

C3=G2+P2G1+P2P1G0+P2P1P0C0

C4=G3+P3G2+P3P2G1+P3P2P1G0+P3P2P1P0C0

C5=G4+P4G3+P4P3G2+P4P3P2G1+P4P3P2P1G0+P4P3P2P1P0C0

C6=G5+P5G4+P5P4G3+P5P4P3G2+P5P4P3P2G1+P5P4P3P2P1G0+P5P4P3P2P1P0C0

C7=G6+P6G5+P6P5G4+P6P5P4G3+P6P5P4P3G2+P6P5P4P3P2G1+P6P5P4P3P2P1G0+P6P5P4P3P2P1P0C0

C8=G7+P7G6+P7P6G5+P7P6P5G4+P7P6P5P4G3+P7P6P5P4P3G2+P7P6P5P4P3P2G1+P7P6P5P4P3P2P1G0+P7P6P5P4P3P2P1P0C0

These are the equations that are considered to generate 8 carries.

These expressions C1-C8 implemented using multiple output domino logic.

8 bit multiple output domino logic for addition to generate carry

These carry are added with sum in full adder.

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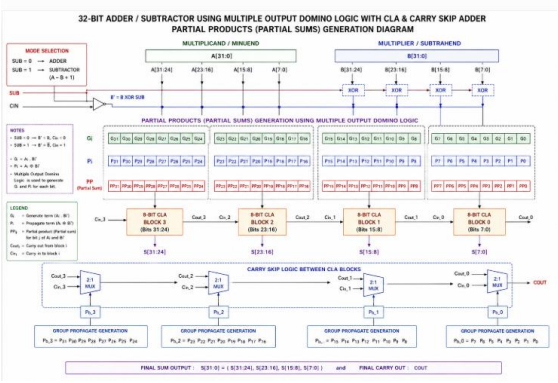


Fig.10: Partial product generation

4. RESULT AND DISCUSSION

Area that is consumed is 986.241micrometer^2

Worst weighted negative slack=0

Total negative slack=0

Power(W):

leakage: 5.87337e-06=3.98%

Internal power: 2.86394e-05=19.39%

Switching:1.13215e-04=76.64%

Total: 1.47727e-04=100%

Cell count 157

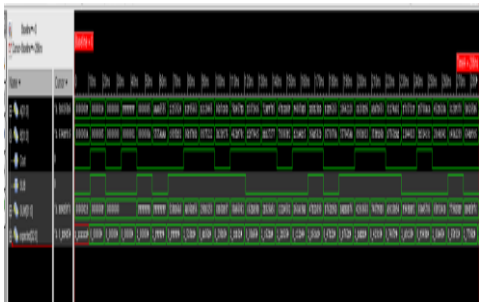


Fig.11: Output Waveform

Synthesis diagram is as shown below.

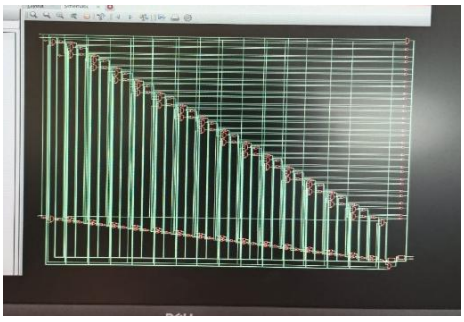


Fig.12: Schematic of synthesis

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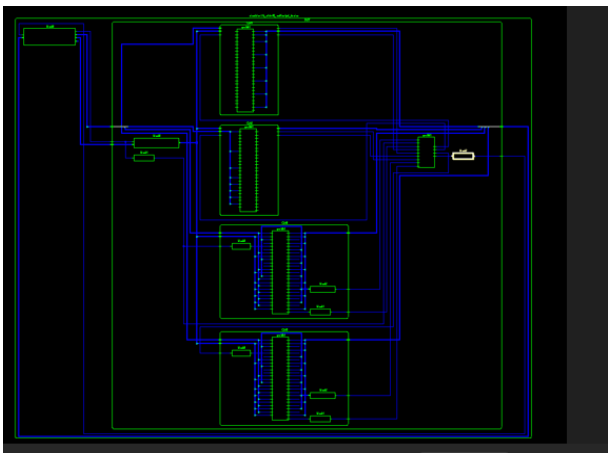
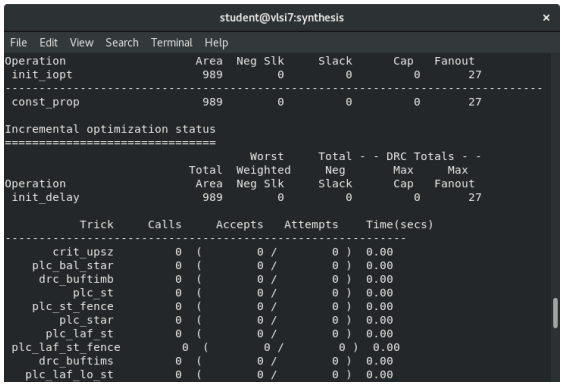


Fig.13: Architecture developed

Area Report

The total area consumed by this architecture using cadence is 986.241micrometer$^{2.}$



```
student@vlsi7:synthesis
File  Edit  View  Search  Terminal  Help
Operation                    Area  Neg Slk     Slack      Cap   Fanout
 init_iopt                    989        0         0        0       27
-------------------------------------------------------------------------------
 const_prop                   989        0         0        0       27

Incremental optimization status
================================
                                  Worst     Total - - DRC Totals - -
                             Total  Weighted     Neg       Max      Max
Operation                    Area  Neg Slk     Slack      Cap   Fanout
 init_delay                   989        0         0        0       27

          Trick     Calls     Accepts   Attempts    Time(secs)
-----------------------------------------------------------------
       crit_upsz         0  (        0 /        0 )  0.00
    plc_bal_star         0  (        0 /        0 )  0.00
     drc_buftimb         0  (        0 /        0 )  0.00
          plc_st         0  (        0 /        0 )  0.00
    plc_st_fence         0  (        0 /        0 )  0.00
         plc_star         0  (        0 /        0 )  0.00
      plc_laf_st         0  (        0 /        0 )  0.00
 plc_laf_st_fence         0  (        0 /        0 )  0.00
     drc_buftims         0  (        0 /        0 )  0.00
   plc_laf_lo_st         0  (        0 /        0 )  0.00
```

Fig.14: Area Report

Gates

Different gates are used in this architecture.

157 instances are used here.

```
-------------------------------------------------------------
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Jul 10 2026  11:08:37 am
  Module:                 adder_subtractor_32bit
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

   Gate    Instances   Area   Library
-----------------------------------------
ADDFX2             2   43.900    slow
AOI21XL           15   68.121    slow
AOI22XL           15   90.828    slow
BUFX2              2    9.083    slow
CLKMX2X2           1    8.326    slow
CLKXOR2X1         15  124.889    slow
CLKXOR2X2         29  263.401    slow
INVXL              1    2.271    slow
MXI2XL            32  193.766    slow
NAND2BXL          15   68.121    slow
NOR2XL            15   45.414    slow
OAI21XL           15   68.121    slow
-----------------------------------------
total            157  986.241         |

     Type      Instances   Area  Area %
----------------------------------------
inverter               1   2.271    0.2
buffer                 2   9.083    0.9
logic                154 974.887   98.8
physical_cells         0   0.000    0.0
----------------------------------------
total                157 986.241  100.0
```

Fig.15: Gate report

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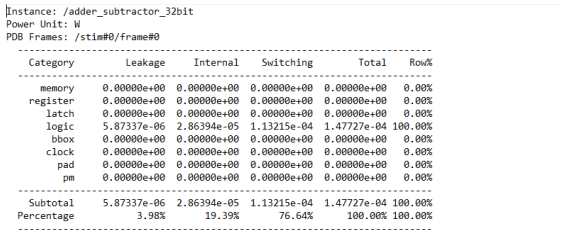
Power

Leakage power is 5.87337e-06(W)=3.98%

Internal power is 2.86394e-05(W)=19.39%

Switching power is 1.13215e-04(W)=76.64%

Total power is 1.47727e-04(W)=100%

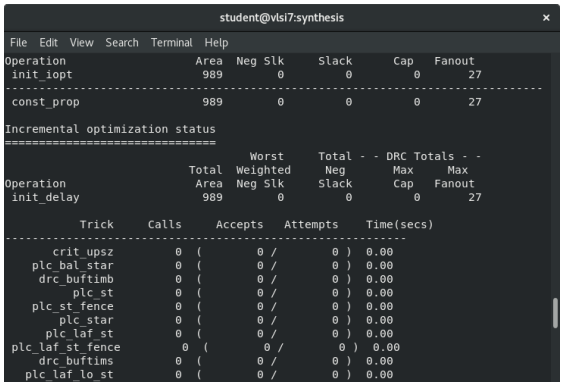


```
Instance: /adder_subtractor_32bit
Power Unit: W
PDB Frames: /stim#0/frame#0
-------------------------------------------------------------------------------
  Category         Leakage     Internal    Switching       Total    Row%
-------------------------------------------------------------------------------
    memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     logic     5.87337e-06  2.86394e-05  1.13215e-04  1.47727e-04 100.00%
      bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
-------------------------------------------------------------------------------
  Subtotal     5.87337e-06  2.86394e-05  1.13215e-04  1.47727e-04 100.00%
Percentage           3.98%       19.39%       76.64%      100.00% 100.00%
-------------------------------------------------------------------------------
```

Fig.16: Power Report

Timing report

The ngative slack is 0.



```
student@vlsi7:synthesis
File  Edit  View  Search  Terminal  Help
Operation                    Area  Neg Slk     Slack      Cap   Fanout
 init_iopt                    989        0         0        0       27
--------------------------------------------------------------------------------
 const_prop                   989        0         0        0       27

Incremental optimization status
================================
                                 Worst     Total - - DRC Totals - -
                           Total Weighted     Neg       Max      Max
Operation                   Area Neg Slk     Slack      Cap   Fanout
 init_delay                   989        0         0        0       27

          Trick     Calls     Accepts   Attempts    Time(secs)
-------------------------------------------------------------
      crit_upsz         0  (        0 /        0 )  0.00
    plc_bal_star        0  (        0 /        0 )  0.00
     drc_buftimb        0  (        0 /        0 )  0.00
          plc_st        0  (        0 /        0 )  0.00
    plc_st_fence        0  (        0 /        0 )  0.00
        plc_star        0  (        0 /        0 )  0.00
      plc_laf_st        0  (        0 /        0 )  0.00
 plc_laf_st_fence       0  (        0 /        0 )  0.00
    drc_buftims         0  (        0 /        0 )  0.00
   plc_laf_lo_st        0  (        0 /        0 )  0.00
```

Fig.17: Timing Report

Table 5: Comparision table

Si.No	Parameter	Reference paper [1]	Proposed paper
1	Area (μm^2)	1223.91	986.241
2	Power (μW)	43.32	147.7

Compared to the reference Paper[1], proposed paper has less area and hence it is efficient in area parameter.

5. FUTURE SCOPE

Layout can be drawn, prediction of reports on area, delay, power, gates can be done using the advanced 4nm technology. Optimization in terms of area, power, gates and delay can be done by optimizing the present architecture.

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BIOGRAPHIES

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