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Design and Area Evaluation of Multiply-and-Accumulate Unit using QCA

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ABSTRACT: For upcoming digital systems, quantum-dot cellular automata (QCA), an emerging nanoscale platform, is expected to provide a potent substitute for the conventional CMOS technology. It is especially appropriate for advanced signal processing applications because of its benefits that include ultra-low power consumption, nano-scopic device dimensions, and the ability to work at very high frequencies, i.e., the high-speed switching characteristic of the technology. The proposed design uses QCA technology to create an energy-efficient MAC unit with a focus on reducing circuit area and power dissipation. QCADesigner version 2.0.3 is used in the design and verification of the suggested architecture to guaranty proper logical functionality. The circuit performance is analyzed under various temperature settings to further assess its practical applicability, showing steady and dependable functioning. The QCAPro tool is used to analyze power consumption, and as per the results the designs uses 50 microwatts of total power. It can be illustrated that a significant gain in power efficiency of around 60% is found, when compared to traditional CMOS-based MAC units, proving its potential for low-power applications. A fundamental computational component of digital signal processing (DSP), the Multiply-Accumulate (MAC) unit serves as the foundation for several real-time processes, including digital filtering, video compression, and voice analysis.

INTRODUCTION

One notable alternative to traditional CMOS technology is Quantum Dot Cellular Automata (QCA), which is often mentioned as a potential replacement for silicon-based transistors. The attractiveness of this paradigm stems from its ability to achieve Terahertz order switching speeds, extreme device integration density up to 1012 devices per square centimeter and low energy consumption [1].

These properties can give an efficiency that CMOS cannot match and provide a strategic path for massive reduction in power consumption in mobile hardware. Also, the inherent strengths of QCA are exceptionally well suited for modern signal and image processing. In communication systems, where the demands of real-time performance and battery preservation are of utmost importance, QCA technology-based architectures provide a revolutionary solution. The basic and the most crucial building block of this architecture is the QCA cell [2]. The Structure of each cell comprises of four distinct wells or "holes," present at corners. These cells are arranged with a precise spacing of 2nm between them [3].

Two mobile electrons that can move between the four holes are present in each cell. Most of these states are intrinsically unstable, even though these electrons may theoretically occupy any of the six possible configurations [4]. The electrons naturally push away from one another due to Coulombic repulsion, looking for a configuration that optimizes their separation. The basic cell structure is represented by Figure-1 [5].

This physical interaction results in two stable, diagonal arrangements:

- Polarization P = +1: Represents a binary logic "1".
- Polarization P = -1: Represents a binary logic "0".

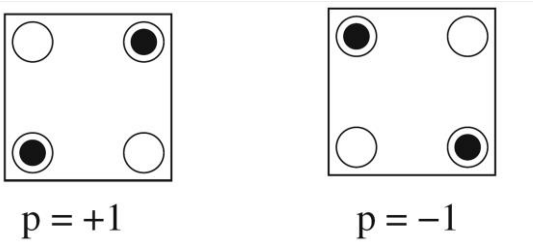


Figure-1: Cell Structure

A QCA cell array can transmit the information as a wire [6]. Figure-2 QCA wires. These wires consist of normal cells placed adjacent to each other, where the electrons from one cell have columbic interaction with the adjacent cell, that results in displacement of the electrons in adjacent cells also [7]. Hence the information propagates through series of such cells, that are aligned in a line. Hence it is usually quoted that information flows in a QCA design without the flow of current.

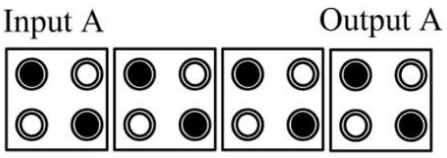


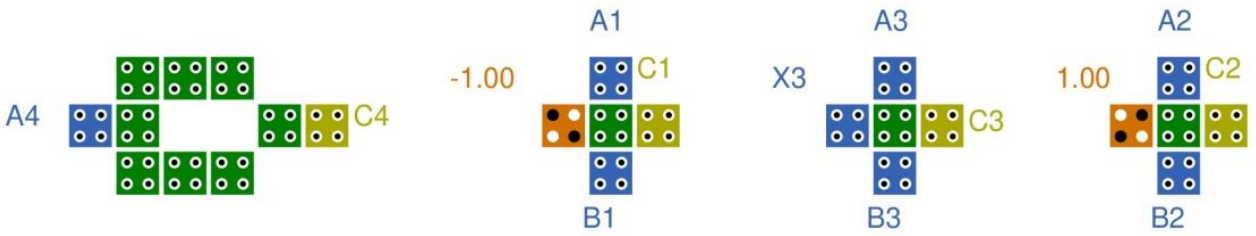
Figure-2: QCA Wire

In the QCA framework, the fundamental logical primitives are the inverter and the majority voter (MV). Unlike traditional CMOS, which relies on NAND or NOR gates, QCA uses these two structures as its primary building blocks [8].

The 3-input Majority Voter (MV3) determines its output based on the state of the majority of its inputs [9]. This gate is highly versatile because it can be programmed to function as standard logic operators:

- AND Gate: By setting one of the three inputs to a permanent logic "0", the output will only be "1" if both remaining inputs are "1".
- OR Gate: By fixing one input to a constant logic "1", the output becomes "1" if either of the other two inputs is "1".

By combining these programmable majority gates with the inverter, which flips the polarization of the cell, QCA technology is capable of synthesizing any complex combinational or sequential digital circuit [10] [11]. This functional completeness allows for the design of everything from simple adders to sophisticated microprocessors using only these basic cell arrangements. Basic cells are as shown in Figure-3 [12 [13].



(a) (b) (c) (d)

Figure-3: QCA Basic blocks (a) Inverter (b) AND gate (c) MV3 Gate (d) OR Gate

Examples of logic gates using above concept is illustrated in Figure-4.

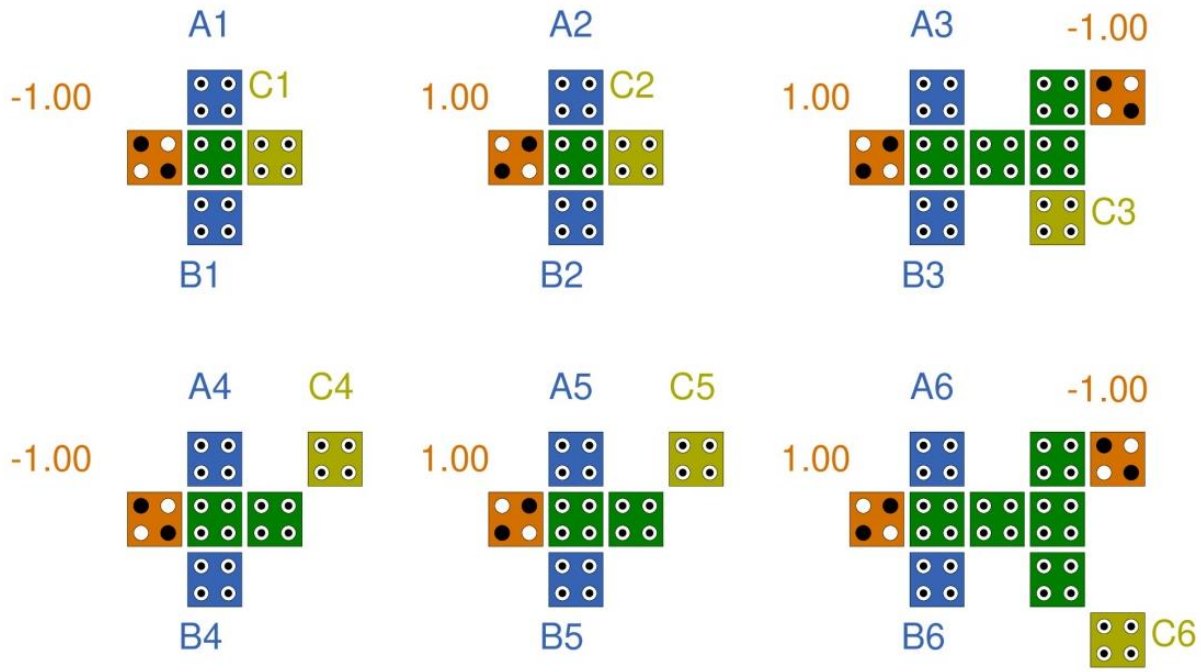


Figure-4: All Logic Gates

QCA CLOCKING-

Clocking in QCA has a more basic physical function, whereas synchronized clock signals are mostly needed for sequential logic in CMOS-based devices. By controlling the potential barriers inside the quantum dots, the clocking mechanism in this nanotechnology is crucial for both data flow control and the amplification of weak input signals [14].

Figure-5 shows Switch, Hold, Release, and Relax are the four discrete, sequential intervals that make up the QCA clocking cycle [15].

The QCA Operation's Four Phases

1. Switch Phase: Cells are initially unpolarized. The cells take on a polarization determined by the effect of their neighbors as potential barriers are progressively elevated.

2. Hold Phase: Electrons are locked into diagonal positions, which are the current positions, when potential barriers reach their maximum limit or value. The cell serves as a reliable input for the subsequent logic stage throughout this particular time.

3. Release Phase: The impact of the cell on surrounding circuit is weakened when the barriers are gradually lowered, allowing the electrons to lose their orientation.

4. Relax Phase: Before the cycle restarts, barriers stay at the lowest level, maintaining the cell at neutral, non-polarized condition.

Despite the fact that several clocking solutions have emerged in recent literature, many confront practical implementation challenges. The development of too long feedback channels, which can affect the timing and layout of intricate signal-processing structures, is a major problem frequently observed in these approaches [16]-[20].

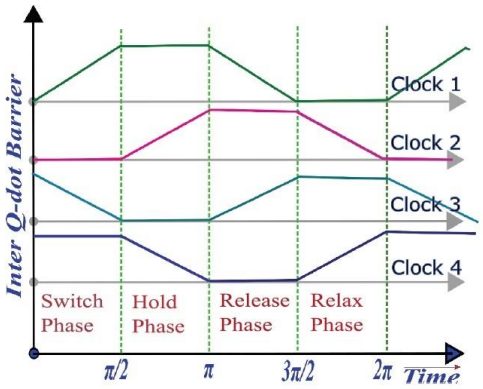


Figure 5: QCA Clocking

DESIGNING OF MAC UNIT-

A dual-function engine called the Multiply-Accumulate (MAC) architecture may perform addition and multiplication in a single processing cycle. High-performance Digital Signal Processing (DSP) and graphics rendering rely heavily on this gear [21]. Three main modules are usually integrated into a MAC unit's fundamental infrastructure: an accumulation register, an adder, and a multiplier, that are illustrated in Figure-6 [22].

The data processing in a typical n-bit setup proceeds in the following order:

1. Multiplication Stage: The multiplier processes two n-bit operands (A and B) to produce a 2n-bit result.

2. Summation Stage: An adder receives the product and adds it to the present sum that is stored in the accumulator.

3. Storage Stage: To be utilized in the next cycle, the updated total is then fed back into the 2n-bit accumulator register.

Until all the terms of data have been analyzed, this cycle continues to run. The traditional method of employing VLSI (Very Large-Scale Integration) techniques to create these components—especially the multiplier—requires a significant amount of physical space and results in high power consumption [23]-[25]. While many researchers have optimized these units for CMOS to improve speed and efficiency, our current approach shifts the implementation of these sub-blocks entirely into the QCA (Quantum-dot Cellular Automata) domain [26].

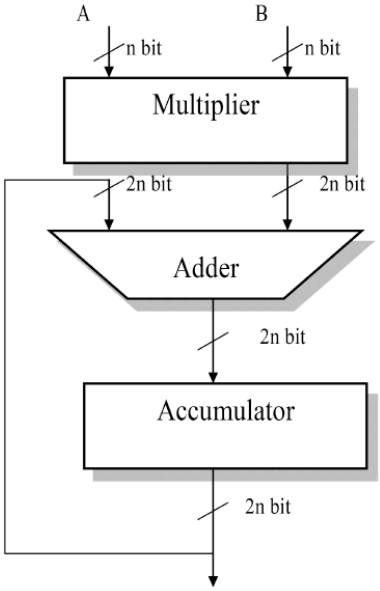


Figure-6: Block Diagram of MAC Unit

By presenting a power-efficient MAC unit, this research work reinforces the current research on QCA-based computing architectures. It emphasizes upon how QCA technology can enable the development of next-generation real-time signal and image processing systems by providing effective, fast processing solutions.

The rapid growth of telecommunications is driving the growing demand for high-velocity computing systems. Three necessary standards are used in the design of these systems: maximizing computing capability, reducing power consumption and physical area occupancy [27] [28].

The Multiply-Accumulator (MAC) unit, an essential unit which plays a vital role in the functioning of mobile and portable multimedia systems. Improving the performance of MAC module is essential as it is a basic and mandatory component of many sub-systems. Although a substantial amount of research has been carried out in improving MAC units, yet most of these efforts depend on conventional CMOS (Complementary Metal–Oxide–Semiconductor) technology [29]-[33].

LITERATURE SURVEY

Ahmadpour et al. [34] used quantum technology to design a multiplier that overcomes the inherent limitations of CMOS and VLSI systems such as high power consumption and slow operating speeds. Although the architecture included essential components such as half adders, full adders, and ripple carry adders to support DSP and systolic array applications, it was quite restrictive. Its practical applicability to complex real-world digital signal processing systems was limited due to its reliance on structures that were not fully optimized for cell count, latency, or area.

Mule and Mande [35] proposed a Data Processing Unit (DPU) based on a linear systolic array for multiple instructions on single data (MISD). The main objective was to minimize the processing errors while maintaining the area and power economy in check by tuning the hardware complexities. The MAC structure was successfully implemented on a Nexys 4 DDR Artix 7 FPGA board and the Xilinx ISE simulations were used to demonstrate the robustness of the framework; however, the implementation was still based on conventional CMOS technology rather than quantum-based alternatives.

To address the thermal and spatial issues of real-time applications such as speech processing and video coding, Gassoumi et al.'s research [36] introduced a QCA-based MAC unit. Their architecture, which was verified using QCADesigner and QCAPro, achieved a remarkable total power consumption of only 2.183 μW, which is 90% less than typical CMOS designs. The design focused on power saving, not on latency and architectural complexity which would hinder its use in high-speed DSP systems, although their outcomes displayed high reliability across various temperatures.

In a subsequent contribution, Gassoumi et al. [37] studied the efficiency of real-time DSP programs using a MAC unit realized with QCA. It consumed 4.03 mW of power, demonstrating better energy and area metrics than traditional hardware. The work was criticized for not investigating circuit scalability and latency, although it confirmed the potential of QCA for signal and picture processing. The difficulties of large-scale system integration were mainly ignored as the emphasis remained on reducing energy consumption.

Combining different multiplier types, such as Wallace tree, DADDA, and array multipliers with row bypassing, is illustrated in the research carried out by Lakshmi et al. [38] which improves performance of MAC architectures. Verilog HDL and the 40 nm Virtex-6 FPGA family were used to examine the effects of various configurations on area and speed. The findings showed that although certain models performed better in terms of area and latency, but these advantages led to minor increases in power consumption and hardware requirement and hence area occupancy.

Campos et al. [15] presented a novel universal, scalable, and efficient (USE) clocking scheme with NAND-NOR-INVERTER (NNI) and majority gates for QCA technology. This method was designed to reduce energy consumption and latency that can speed up the components in systems, like SRAMs and multipliers. A significant step towards the creation of effective sub-blocks using QCA was made with the 4 × 4 Vedic multiplier, which significantly reduced cell count and area by more than 60% and 80%, respectively.

Design of a 32-bit reversible MAC unit architecture aimed to reduce quantum cost and garbage outputs by Vamsi et al. [39]. The research work depicted increase in the effectiveness of DSP devices by using a 64-bit reversible PIPO unit and a Radix-16 Booth-encoded Wallace tree multiplier. Although the design was successfully synthesized using the Cadence RTL compiler and installed on a Xilinx Virtex 7 FPGA, it is essentially grounded in CMOS-based technology, which left the transfer to genuine QCA logic as a next step.

Abrar and Chavan [40] proposed an area efficient design of a 16-bit Multiply-Accumulate unit (MAC) implemented using QCA. It is designed using an area efficient novel 1-bit Full adder incorporated in a 16-bit Parallel binary adder and 8-bit multiplier modules. The design proposed by the authors for 1-bit adder has reduced the cell count by 9.09% and area by 33.33%.

Asthana et al. [41] also proposed design of a multiply-accumulate operation (MAC) unit, that can be used to reduce the processing time of the central processing unit (CPU) or arithmetic logical unit (ALU) of a sub-system. In this research work the MAC unit has been designed to reduce the complexity of the cross-connect circuits. The complete circuit has been implemented using standard AND gate and full adder, in quantum dot cellular automata, to reduce the power dissipation and cell area. This research work comprises of designing a low-power MAC unit circuit, that can be used with cross-connect networks with M parallel operations and with N size networks to make M × N operations per unit time. The power dissipation has been computed as 2.416x10−9 W.

PROPOSED DESIGN

In a Multiply-and-Accumulate unit we compute the product of two numbers added to the previously stored sum. Such modules are essential in design of digital signal processing systems that involve computations with matrices, convolution etc. such designs can be achieved through the integration of multiplier followed by accumulator.

Generally, the design is supposed to comprise of a multiplier, whose output is stored in memory unit, and then the same is fed to an ALU which ads the present output of the multiplier to the previously stored output. Thus, achieving addition of two values obtained- one resulting from multiplication of present inputs, and the other resulting from previously multiplied data.

In QCA, the units can be combined in the sequence as specified by the design. But the vital role is played by sequencing of clock zones for proper signal flow. This can be achieved by designing the multiplier units in one clock zone, followed by designing adder in the next clock zone. These adders give the accumulated output, as expected in a MAC design.

In the proposed research work, a binary MAC is suggested to be designed, which comprises of a shift register as binary multiplier. In this multiplier, the fundamental of binary multiplication is utilized, where a binary number shifted left is considered as multiplication by 2. The shifted value is fed as input to the binary adder that adds the shifted data with previous data. Previous data is delayed by one complete clock cycle, instead of storing it in any memory unit. This delayed addition results in minimizing design hardware, as the requirement of memory unit for storage is eliminated.

The block diagram of the concept is as illustrated in Figure-6. The same is designed using QCA and tested. Thus, the obtained simulation results are verified and found to be correct.

RESULTS

Simulation of MAC unit was carried out in a step-wise process. First, the basic blocks like logic gates and adders were designed. These designs were optimized for their performance in terms of area occupied and number of cells required in the design. The most efficient design was selected as the final module to be included in the realization of MAC unit.

For simulation of the designs, the simulation tool selected was QCADesigner with version 2.0.3. the simulation engine set-up was tested for “Coherence Vector” type as well as “Bistable Simulation” type. Results obtained in both the cases are identical. Since the results are simulated comparatively faster in Bistable Simulation, hence the choice. Considering Bistable Simulation, the parameters set-up are-

Simulation Engine : Bistable Approximation

Simulation Order : Random

Clock High : 9.8 e-022

Clock Low : 3.8 e-023

Clock shift : 0

Layer Separation : 11.5nm

Maximum iterations per sample : 100

The simulation results are tested for various combinations of inputs. Figure-7 illustrates an adder design along with its simulation results illustrated in Figure-8. The design of multiplier is illustrated in Figure-9 along with its simulated results in Figure-10. The design is tested for various other combinations of inputs also, and is found to be accurate in terms of values and delays.

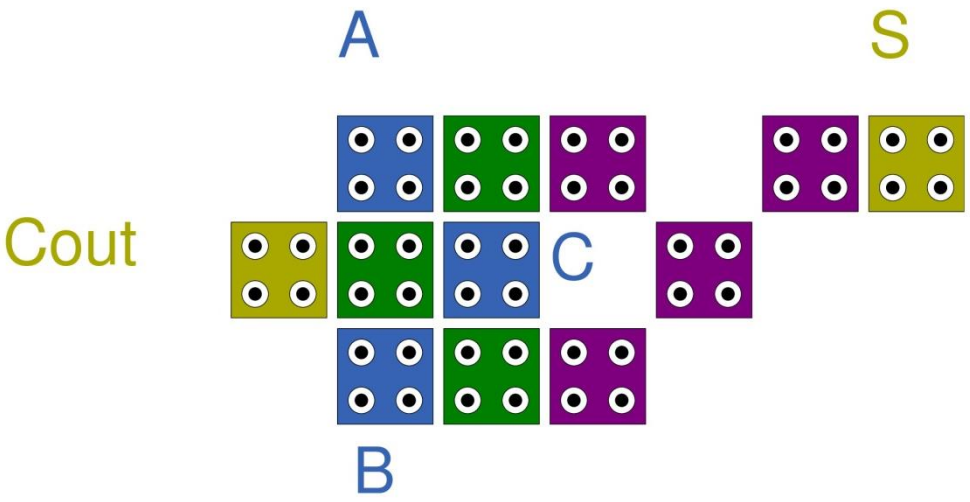


Figure-7: Adder designed using QCA

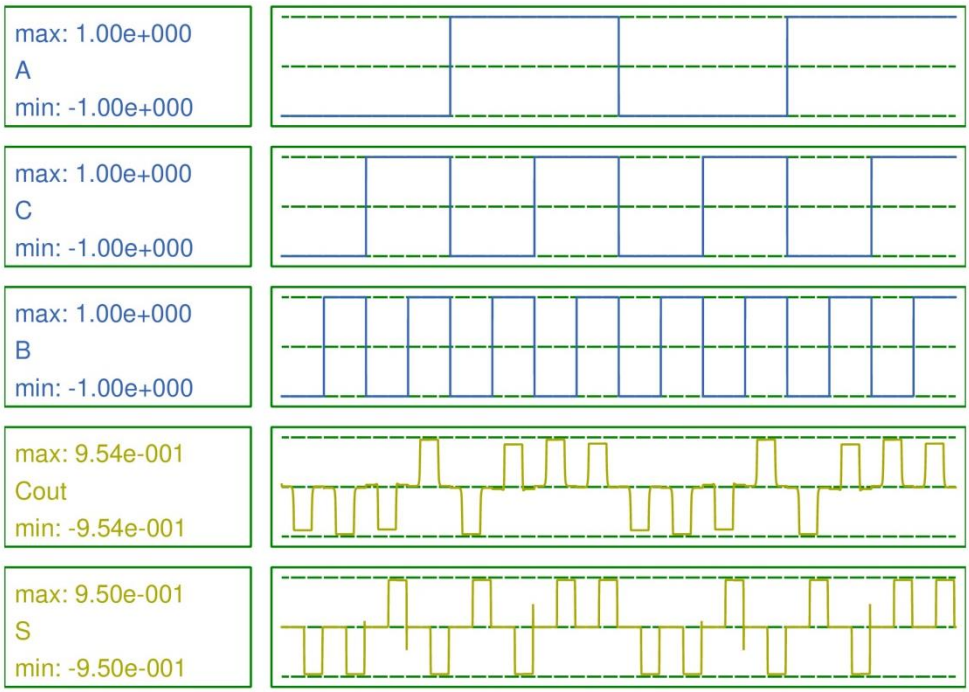


Figure-8: Simulation Results of QCA-Adder

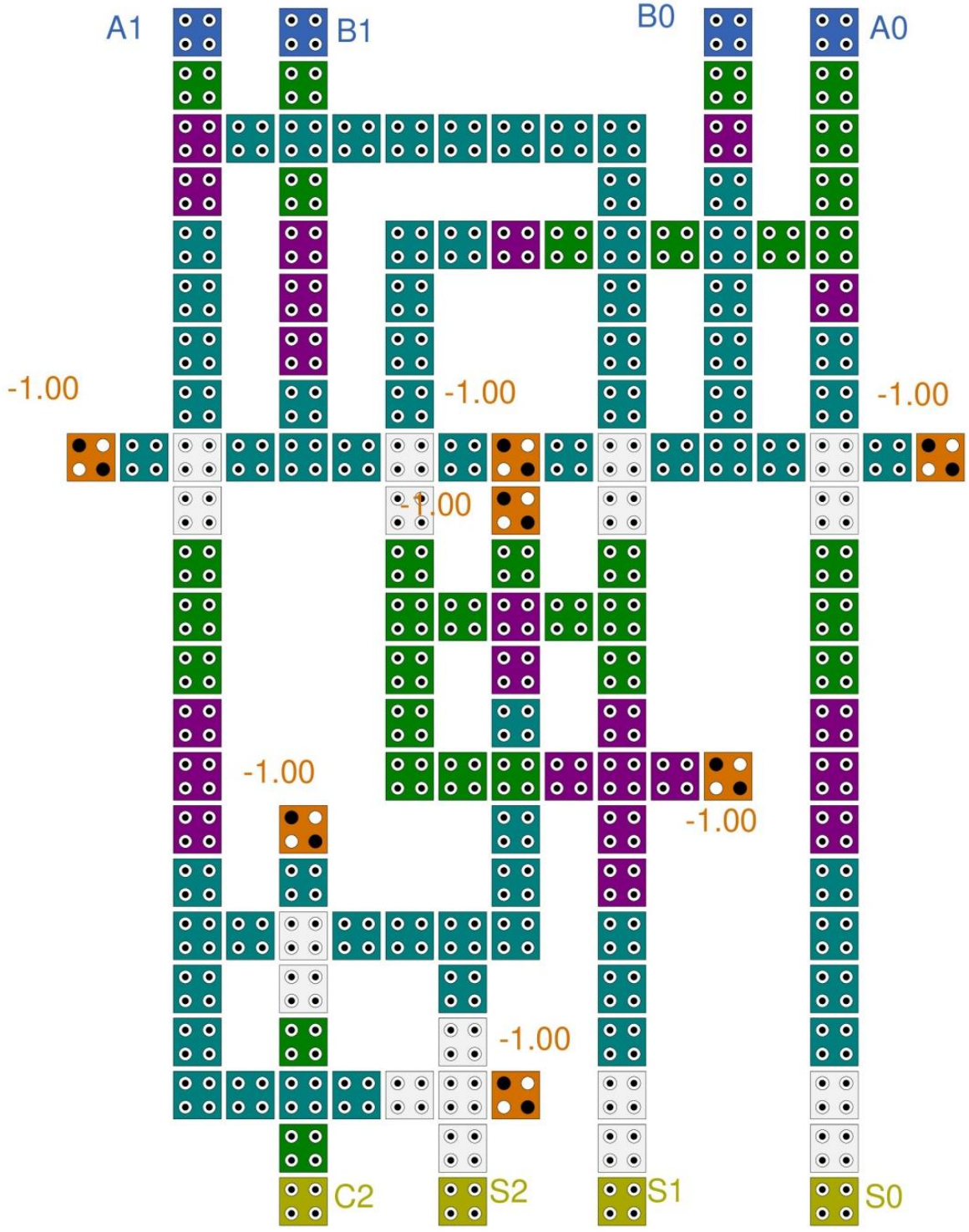


Figure-9: QCA layout of Multiplier

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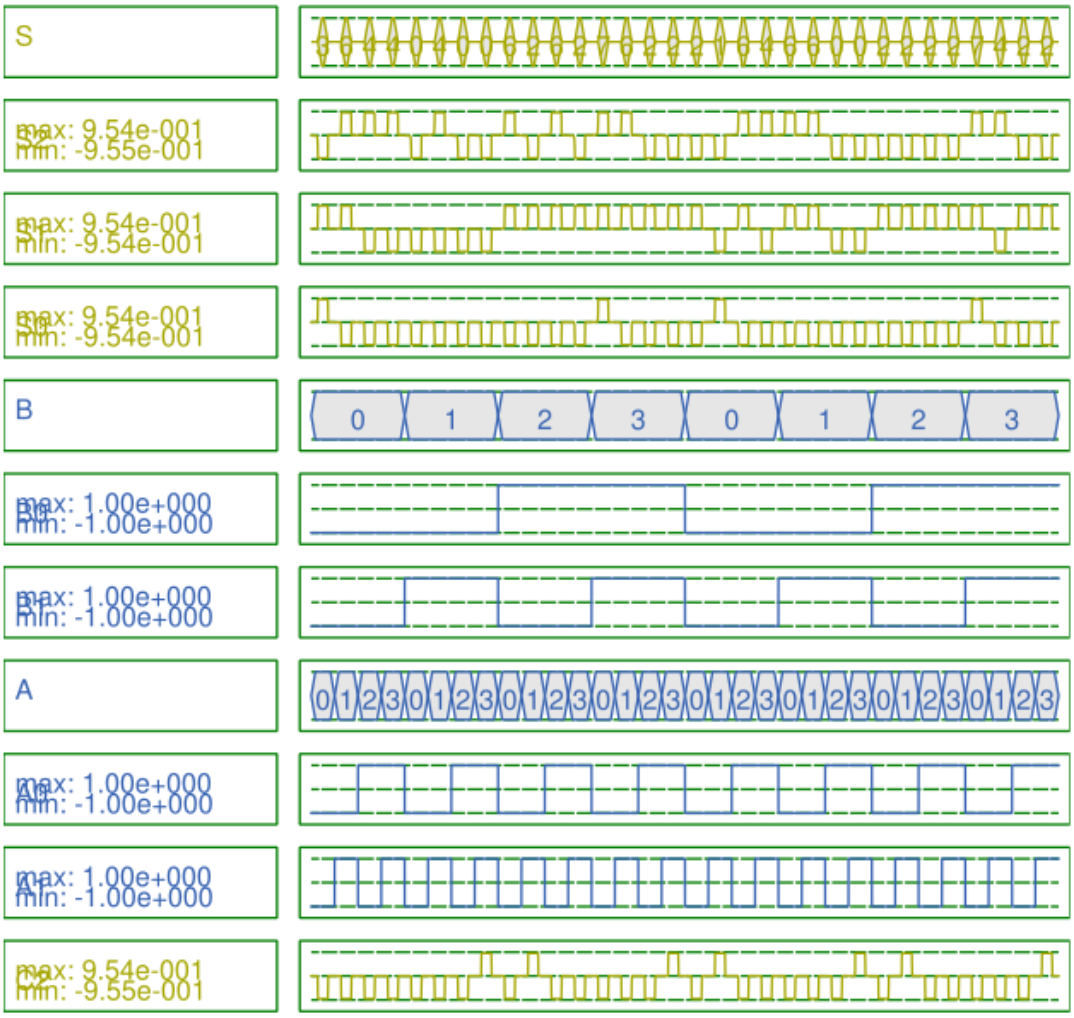

Figure-10: Simulation Results of Multiplier

The above multiplier is utilized to build a MAC unit. The proposed multiplier, along with the adder design and its integration with complete layout, is as illustrated in Figure-9. Comparing the proposed design with various other designs, it is evident that the proposed design serves to be efficient in terms of area as well as number of cells required. Thus, making the proposed design a desirable one, in integrating it in applications like signal processing and communication.

As application-based circuit designs are emerging, the need for an efficient MAC unit is raising every day. With the proposed design of MAC, many such applications can be realized with least area occupancy and high-performance efficiency. Thus, making the proposed design of MAC unit as the most efficient one designed in present days.

CONCLUSION

In the proposed design of MAC unit structured using basic blocks like adders and multipliers, a modular approach of designing is followed, where in various blocks are designed first and then interconnected together to form an overall MAC functioning block. The proposed design provides efficient performance area-wise along with least number of cells required to implement the design. These advantages make the proposed design of MAC most suitable for applications like signal processing and communication devices, where real time processing is required along with minimal area occupancy. The proposed design proves to reduce the area by _____% and cells required by ___%. Thus, making the design utilize clocking phases efficiently and synchronize the functions in an optimum way.

REFERENCES

[1] C.S. Lent, J.P. Bird, et al., Quantum-Dot Cellular Automata, Electron Transport in Quantum Dots, Springer, Boston, MA, 2003, doi:10.1007/978-1-4615-0437-5_10

[2] W. Liu, L. Lu, M. O'Neill, E.E. Swartzlander, A first step toward cost functions for Quantum-Dot Cellular Automata Designs, IEEE Trans. Nanotechnol. 13 (3) (May 2014) 476–487, doi:10.1109/TNANO.2014.2306754.

[3] Tougaw, P. and Lent, C. (1994) Logical Devices Implemented Using Quantum Cellular Automata. Journal of Applied Physics, 75, 1818-1825. http://dx.doi.org/10.1063/1.356375

[4] Abbas Shahini Shamsabadi, Behrouz Shahgholi Ghahfarokhi, Kamran Zamanifar, Naser Movahedinia, Applying inherent capabilities of quantum-dot cellular automata to design: D flip-flop case study, Journal of Systems Architecture, Volume 55, Issue 3, 2009, Pages 180-187, ISSN 1383-7621, https://doi.org/10.1016/j.sysarc.2008.11.001

[5] Sen, Dr. Bibhash & Rajoria, Ayush & Sikdar, Biplab. (2013). Design of Efficient Full Adder in Quantum-Dot Cellular Automata. The Scientific World Journal. 2013. 250802. 10.1155/2013/250802.5.

[6] Chakrabarty, Ratna & Mandal, Niranjan. (2021). Realization of combinational logic circuits using standard functions in quantum dot cellular automata. Nanosystems: Physics, Chemistry, Mathematics. 12. 583-597. 10.17586/2220-8054-2021-12-5-583-597.

[7] Pathak, Nirupma & Misra, Neeraj Kumar & Bhoi, Bandan & Kumar, Santosh. (2021). Optimization of Parameters of Adders and Barrel Shifter Based on Emerging QCA Technology. Radioelectronics and Communications Systems. 64. 535-547. 10.3103/S0735272721100022.

[8] Sayedsalehi, Samira, Mohammad Hossein Moaiyeri and Keivan Navi. "Novel Efficient Adder Circuits for Quantum-Dot Cellular Automata." Journal of Computational and Theoretical Nanoscience 8 (2011): 1769-1775.

[9] Liolis, O., Mardiris, V. A., Karafyllidis, I. G., Cotofana, S., & Sirakoulis, G. C. (2023). Methodology for automated design of quantum-dot cellular automata circuits. IEEE Open Journal of Nanotechnology, 4, 1-13

[10] Sen, Dr. Bibhash & Rajoria, Ayush & Sikdar, Biplab & Miah, Shahajan. (2013). Design of Efficient Full Adder in Quantum-Dot Cellular Automata. The Scientific World Journal. 2013. 250802. 10.1155/2013/250802.

[11] Tougaw, D., & Will, J. D. (2020). Designing a Turing-complete cellular automata system using quantum-dot cellular automata. Journal of Computational Electronics, 19(3), 1145–1152. https://doi.org/10.1007/s10825-020-01518-1

[12] Aliabadian, Ramin & Golsorkhtabar, Mehdi & Rasouli Heikalabad, Saeed & Sohrabi, Mohammad. (2023). Design of a reversible ALU using a novel coplanar reversible full adder and MF gate in QCA nanotechnology. Optical and Quantum Electronics. 55. 10.1007/s11082-022-04382-4.

[13] Majeed, Ali, and Milad Khosroshahy. "HIGHLY EFFICIENT INVERTER BLOCKS IN QCA TECHNOLOGY". Kufa Journal of Engineering, vol. 15, no. 2, May 2024, pp. 16-26, https://doi.org/10.30572/2018/KJE/150202.

[14] Vankamamidi, V., Ottavi, M., & Lombardi, F. (2007). Two-dimensional schemes for clocking/timing of qca circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 27(1), 34–44. https://doi.org/10.1109/TCAD.2007.907020

[15] Campos, C. A. T., Marciano, A. L., Neto, O. P. V., & Torres, F. S. (2015). Use: A universal, scalable, and efficient clocking scheme for qca. IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, 35(3), 513–517. https://doi.org/10.1109/TCAD.2015.2471996.

[16] Goswami, M., Mondal, A., Mahalat, M. H., Sen, B., &Sikdar, B. K. (2019). An efficient clocking scheme for quantum-dot cellular automata. International Journal of Electronics Letters, 8(1), 83–96. https://doi.org/10.1080/21681724.2019.1570551

[17] Wang, L., Xie, G., Zhu, R., & Yu, C. (2019). An optimized clocking scheme for nanoscale quantum-dot cellular automata circuit. In 2019 IEEE 14th international conference on nano/micro engineered and molecular systems (nems), Bangkok, Thailand (pp. 336–341). IEEE.

[18] Deng, F., Xie, G., Cheng, X., Zhang, Z., & Zhang, Y. (2019). CFE: A convenient, flexible, and efficient clocking scheme for quantum-dot cellular automata. IET Circuits, Devices & Systems, 14(1), 88–92. https://doi.org/10.1049/iet-cds.2019.0096.

[19] Pal, J., Pramanik, A. K., Goswami, M., Saha, A. K., &Sen, B. (2022). Regular Clocking based Emerging Technique in QCA Targeting Low Power Nano Circuit. International Journal of Electronics, 109(9), 1550–1572. https://doi.org/10.1080/00207217.2021.1972473

[20] C. S. Lent and B. Isaksen, "Clocked molecular quantum-dot cellular automata," in IEEE Transactions on Electron Devices, vol. 50, no. 9, pp. 1890-1896, Sept. 2003, doi: 10.1109/TED.2003.815857.

[21] Safaiezadeh, Behrouz & Haghparast, Majid & Kettunen, Lauri. (2023). Novel Efficient Scalable QCA XOR and Full Adder Designs. 10.48550/arXiv.2302.13946.

[22] Ambika, G. & Shanthala, G. & Sharan, Dr & Talabattula, Srinivas. (2018). An Optimized Design of Complex Multiply-Accumulate (MAC) Unit in Quantum Dot Cellular Automata (QCA). 10.1007/978-981-10-7656-5_11.

[23] Rao, Y. N., Raju, G. S., & KrishnaRaja, P. V. (2014). Design and Performance Evaluation of High Speed MAC Unit with Parallel Pipeline Technology. International Journal of Computer Applications, 106(4), 30-34.

[24] Babaie, Shahram, Ali Sadoghifar and Ali Newaz Bahar. “Design of an Efficient Multilayer Arithmetic Logic Unit in Quantum-Dot Cellular Automata (QCA).” IEEE Transactions on Circuits and Systems II: Express Briefs 66 (2019): 963-967.

[25] Sharma, Vijay. (2021). Optimal design for 1:2 demultiplexer using QCA nanotechnology with energy dissipation analysis. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields. 34. 10.1002/jnm.2907.

[26] Huang, Xiaoping, Wen-Jung Liu and Belle W. Y. Wei. “A high-performance CMOS redundant binary multiplication-and-accumulation (MAC) unit.” IEEE Transactions on Circuits and Systems I-regular Papers 41 (1994): 33-39.

[27] Sasamal T. N., Singh A. K., and Ghanekar U.: “Design of QCA-based D Flip flop and memory cell using rotated majority gate.” In: BijayaKetanPanigrahi, Munesh C. Trivedi, Krishn K. Mishra, ShaileshTiwari, and Pradeep Kumar Singh (eds) Smart Innovations in Communication and Computational Sciences. Springer, 233–247 (2019).

[28] Walus, Konrad & Dysart, T.J. & Jullien, Graham & Budiman, Roes. (2004). QCADesigner: A Rapid Design and Simulation Tool for Quantum-Dot Cellular Automata. Nanotechnology, IEEE Transactions on. 3. 26 - 31. 10.1109/TNANO.2003.820815.

[29] Safaiezadeh, B., Mahdipour, E., Haghparast, M. et al. Design and simulation of efficient combinational circuits based on a new XOR structure in QCA technology. Opt Quant Electron 53, 684 (2021). https://doi.org/10.1007/s11082-021-03294-z.

[30] Liolis, Orestis & Mardiris, Vassilios & Karafyllidis, Ioannis & Cotofana, Sorin & Sirakoulis, Georgios. (2022). Methodology for Automated Design of Quantum-Dot Cellular Automata Circuits. IEEE Open Journal of Nanotechnology. PP. 1-10. 10.1109/OJNANO.2022.3223413.

[31] Chetti, Smita C. and Omkar Yatgal. “QCA: A Survey and Design of Logic Circuits.” Global Transitions Proceedings (2022)

[32] Smita C. Chetti, M. B. Veena, "Conceptualization and Design of 8-Bit SRAM Using Quantum Dot Cellular Automata," SSRG International Journal of Electrical and Electronics Engineering, vol. 11, no. 1, pp. 14-27, 2024. Crossref, https://doi.org/10.14445/23488379/IJEEE-V11I1P103.

[33] Alharbi, M.; Edwards, G.; Stocker, R. Hybrid Quantum-Dot Cellular Automata Nanocomputing Circuits. Electronics 2024, 13, 2760. https://doi.org/10.3390/electronics13142760

[34] Ahmadpour, Seyed-Sajad & Zohaib, Muhammad & Rasmi, Hadi & Jafari Navimipour, Nima. (2026). High-performance and low-power quantum-dot-based multiply–accumulate design for next-generation supercomputing platforms. The Journal of Supercomputing. 82. 10.1007/s11227-025-08220-8.

[35] Mule, Priya & Mande, Sudhakar. (2023). Design and Performance Analysis of FPGA based DPU using MAC Unit. 1-6. 10.1109/I2CT57861.2023.10126363.

[36] Gassoumi, Ismail, Lamjed Touil and Bouraoui Ouni. "Design of Efficient Quantum-Dot Cellular Automata (QCA) MAC Unit." 2018 30th International Conference on Microelectronics (ICM) (2018): 1-4.

[37] Gassoumi, Ismail, Lamjed Touil and Bouraoui Ouni. "Design of efficient quantum Dot cellular automata (QCA) multiply accumulate (MAC) unit with power dissipation analysis." IET Circuits Devices Syst. 13 (2019): 534-543.

[38] Lakshmi, Vijaya & Reuben, John & Pudi, Vikramkumar. (2021). A Novel In-Memory Wallace Tree Multiplier Architecture Using Majority Logic. IEEE Transactions on Circuits and Systems I: Regular Papers. 69. 1148-1158. 10.1109/TCSI.2021.3129827.

[39] Reddy, V. R., & Reddy, V. R. (2026). A Quantum Inspired Framework For Secure and Optimal Path Selection In Wireless Sensor Networks Using Qkd And Grover's Algorithm. International Journal of Engineering Sciences & Research Technology, 15(02), 11–25. https://doi.org/10.64149/j.ijesrt.15.2.11-25

[40] Vamsi, Hari Sai Ram, Kumar Reddy, C. Babu and Narasimha Murty. "Design of reversible logic based 32-bit MAC unit using radix-16 booth encoded wallace tree multiplier." 2018 International Conference on Computer Communication and Informatics (ICCCI) (2018):1-6.

[41] Hamadou A., Hassane A. A. I., Naroua H., Hama A. N. A., Salissou A. S., Chaharou I. M. L. (2026). A Comparative Experimental Study of Index Performance In Mongodb And Postgresql. International Journal of Engineering Sciences & Research Technology, 15(4), 22-31 https://doi.org/10.64149/j.ijesrt.15.4.22-31

[42] Abrar, Mohammed and Arunkumar P. Chavan. "Design of Area Efficient Multiply Accumulator Unit in Quantom Dot Cellular Automata (QCA)." Lecture Notes in Electrical Engineering (2021): n. pag.

[43] Asthana, Amit, Anil Kumar, Sumita Mishra, Preeta Sharan and Md. Tabrez. "Design of Single Bit Low Power Multiply Accumulate (MAC) Unit Using Quantum Dot Cellular Automata." 2021 8th International Conference on Computing for Sustainable Global Development (INDIACom) (2021): 725-729.